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Lab Report 4

Introduction:

The purpose of this lab was to study the time delay between input and output of a logic gate, two different logic gate’s delay, or propagation delay was studied.

Team Member Responsibilities:

This lab was done alone.

List of Materials:

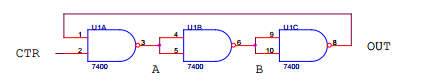
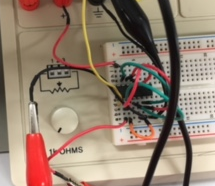
ELENCO Analog kit Oscilloscope digital power supply assorted wires and cables

7400 Quad 2 input NAND chip CD4011BC Quad 2 input NAND chip

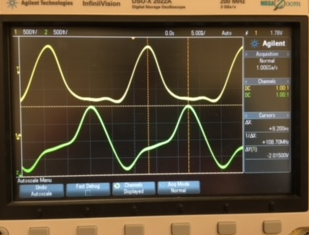
Procedure:

Part I:

The ELENCO analog kit was powered up, the supply voltage to the chip was set at 5v. The 7400 Quad 2 input NAND chip was powered with this 5v input.

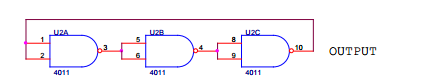
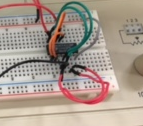
 

This figure above was used to wire the 7400 Quad 2 input NAND chip, three of the four logic gates on the chip were used the output from the last gate was wired back into the input of the first gate thus creating an endless loop, and a sin function. The other input was from a built in logic gate on the ELENCO kit set to always input Logical one. The Oscilloscope was attached using a cable at one input and one output of one of the logic gates. Then the period and time delay was measured from high to low and low to high.

This image to the left is what the Oscilloscope should look like

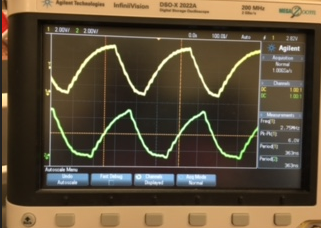
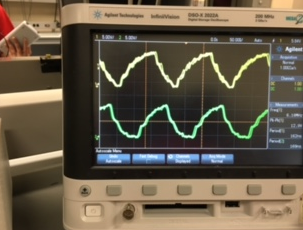
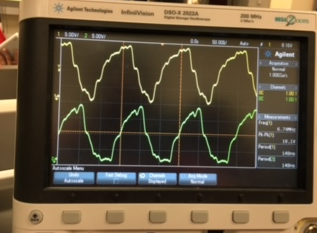
Part II:

The ELENCO analog kit was powered up, the supply voltage using and digital power supply powered the CD4011BC Quad 2 input NAND chip. The digital power supply input was changed from 5v to 10v to 15v depending on what was needed.

The figure above was used to wire the D4011BC Quad 2 input NAND chip , three of the four logic gates on the chip were used the output from the last gate was wired back into the input of the first gate thus creating an endless loop, and a sin function. The Oscilloscope was attached using two cables at one input and one output of two of the logic gates. Then the period and time delay was measured from high to low and low to high. This process was repeated for when the chip was 10v and 15v.

The outputs should look like:

5v 10v 15v

QUESTIONS:

I. SN7400 Datasheet:

1. Determine the average propagation delay pd t for the 7400 NAND gate from its

datasheet. Consider both typical and maximum values.

Derived value from data sheet was 13.75ns

(assuming testing conditions RL = 400 Ω, CL = 15 pF)

|  |  |  |
| --- | --- | --- |
| High to Low | High to low | AVG(ns) |
| TYP | 11 | 7 | 9 |
| Max| 22 | 15 | 18.5 |
| Average Propagation Delay Time | | 13.75 |

II. Propagation Delay Measurement – Theory:

1. Determine the times t1, t2, t3, t4, t5, and T of Fig. 2 in terms of the low-to-high

propagation time PLH t and the high-to-low propagation time PHL t .

High to Low = 7 Low to High = 11

t1 = 11ns

t2 = 11+7 = 18ns

t3 = 18 + 11 = 29ns

t4 = 29 + 7 = 36ns

t5 = 36 + 11 = 47ns

T = 47+7 = 54ns

2. Derive a formula that relates the time period T of the fundamental period of the

oscillations to the average propagation delay pd t .

T(period) = 6 x t(pd, avg propagation delay)

III. Propagation Delay Measurement – Practice:

1. Accurately sketch one complete cycle of oscillation.

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1. Experimentally measure the time period of the fundamental period of the

oscillations.

Time period measured using the oscillator scope was 22.2ns

1. Determine the experimental average propagation delay pd t .

Experimental value was 9.05ns

( 13.2 + 4.9 ) / 2 = 9.05

IV. CD4011 NAND Gate:

1. Determine the average propagation delay pd t for the 4011 NAND gate from its

datasheet with supply voltages of 5V, 10V and 15V. Consider both typical and maximum values.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| voltage | math | Avg(ns) | Typ+Max avg | Avg Prop. Delay(ns) |
| 5v TYP | (125 + 60)/2= | 82.5 | (82.5 +225 )/2 = | 153.75 |
| 10v | (60 + 50)/2= | 55.0 | (55 + 110)/2 = | 82.5 |
| 15v | (45 + 40 )/2= | 42.5 | (42.5+85)/2 = | 63.75 |
| 5v MAX | (250+200)/2 | 225 |  |  |
| 10v | (120+100)/2 | 110 |  |  |
| 15v | (90+80)/2 | 85 |  |  |

2. Determine the experimental average propagation delay pd t for the three supply

voltages.

|  |  |  |  |
| --- | --- | --- | --- |
| voltage | High to Low | Low to High | avg |
| 5v | 116 | 114 | 115 |
| 10v | 43 | 36 | 39.5 |
| 15v | 42 | 34 | 38.5 |

V. Conclusions:

1. Discuss how the average propagation delay pd t derived from the datasheet for

the 7400 and 4011 NAND gate compares to your experimentally determined

value.

For 7400 gate, the experimental avg propagation delay value was 9.05ns while the derived avg propagation delay is 13.75ns, there is a 4.7ns difference in it because the derived value accounts for the max propagation delay if only the TYP propagation delay was calculated it would be 9ns delay which is nearly identical to my data.

For the 4011 gate, the experimental avg propagation for 5v, 10v, 15v were respectively 115ns, 39.5ns, 38.5ns. The derived avg propagation for 5v, 10v, 15v were respectively 153.75ns, 82.5ns, 63.75ns. My data while not matching the calculated data, it did follow the same trend of having smaller and smaller delays when voltage power to the chip increased.

2. Discuss how the average propagation delay pd t for the 4011 NAND gate varies

as a function of supply voltage.

As the supply voltage increase to the 4011 NAND gate the avg propagation delay decreases, it is an inverse relationship (t = 1/v \* constant)

3. Discuss how the average propagation delay pd t compares for TTL and CMOS

families of logic.

If both gates are using a 5v supply then the TTL family is clearly supieror if a smaller delay time window is desired, however if a circuit is dealing with higher and higher voltages the CMOS family of logic might be better suited since it’s avg delay decreases with more power.

4. Discuss how you could experimentally determine the average propagation delay

pd t for other inverting gates such as the NOT and NOR gates.

For the NOT gate simply set up loop three or more, as long its and odd number of gates together with the last output go into the input of the first one, the same concept works for the NOR gates.